duced to the row latch **2**. The cycle of t_{21} operates identically to that of t_2 in FIG. **4**, in which a column address in the address signal **A0–A9** is introduced to the column latch **4**.

In the cycle of t_{22}, a column address in the address signal **A0–A9** is introduced again to column latch **4**, as in the t_{21} cycle. Namely, only column addresses are introduced successively. The cycle of t_3 is identical to that of t_3 in FIG. **4** and the explanation thereof is omitted.

In this manner, for the page mode read (or write) cycle, a row address in the address signal **A0–A9** is introduced to the row latch **2**, and thereafter column addresses in the address signal **A0–A9** are introduced successively to the column latch **4**.

According to the foregoing embodiment, a semiconductor memory which is based on address multiplexing and is operative on a single clock signal can be accomplished by merely adding a few latch circuits and associated control circuit to the conventional MOS dynamic RAM.

Although the foregoing embodiment is the case of writing and reading for one-bit data, this invention is not confined to this case, but the arrangement for dealing with multiple-bit data can also be accomplished. Although in the foregoing embodiment an external row address is introduced for the refresh address, it is also possible to provide an internal address counter, thereby eliminating the need of the external address input.

We claim:

1. A semiconductor memory chip, comprising:

a memory cell array;

means of receiving an address signal having a row address signal and a column address signal in such a manner that the row address signal is received first and then the column address signal is subsequently received;

means of communication with the outside for inputting and outputting data to and from said memory cell array;

means for receiving a clock signal having a series of clock pulses;

means for receiving a chip select signal from the outside which represents that the semiconductor memory is selected;

means responsive to the clock signal and the chip select signal for generating a row address set signal and a column address set signal, wherein the row address set signal is generated under a circumstance where the semiconductor memory receives a firstly occurred clock pulse of the series of the clock pulses of the clock signal while the chip select signal is being provided to the semiconductor memory, and wherein the column address set signal is generated under a circumstance where the semiconductor memory receives a subsequent clock pulse while the chip select signal is being provided to the semiconductor memory;

means responsive to the row address set signal for setting the address signal from the means of receiving as the row address signal and for providing the memory cell array with the set row address signal; and

means responsive to the column address set signal for setting the address signal from the means of receiving as the column address signal and for providing the memory cell array with the set column address signal.

2. A semiconductor memory according to claim **1**, wherein said memory cell array is of the dynamic type which requires a refresh operation, and [wherein said control means controls the refresh operating] *further including means for conducting the refresh operation* based on said clock signal.

3. A semiconductor memory according to claim **1** operable with a page mode, wherein the means for generating further generates a continuous series of column address set signals in synchronism with said clock signal as long as the chip select signal is provided, whereby memory access to a plurality of memory cells belonging to the same row is continuously performed in accordance with the series of the column address set signals.

4. A semiconductor RAM chip, comprising:

an address input terminal for receiving an address signal having row and column addresses time multiplexed;

a chip select input terminal for receiving a chip select signal to indicate the selection of the semiconductor RAM;

a clock input terminal for receiving a clock having a single periodic succession of clock pulses;

a memory cell array;

a data output terminal connected to said memory cell array to output data from said memory cell;

a data input terminal connected to said memory cell array for receiving data for said memory cell;

a row address decoder having a row address input and an output connected to said memory cell array;

a column address decoder having a column address input and an output connected to said memory cell array; and

means for receiving the multiplexed address signal from said address input terminal and the clock from said clock input terminal, and for outputting the row address to the input of the row address decoder separate from the column address and outputting the column address to the input of the column address decoder separate from the row address in response to only the clock when the chip select signal at said chip select input terminal indicates the selection of the semiconductor RAM.

5. The semiconductor RAM of claim **4**, further comprising:

a column selection circuit operatively connected between said memory cell array and each of said data output terminal, data input terminal and means for receiving and outputting;

an enable input terminal for receiving an enable signal to indicate a selection of one of a write operation and a read operation;

said column selection circuit including means responsive to said enable signal for controlling the data connection between said memory cell array and each of said data input terminal and data output terminal;

a latch operatively connected between said data output terminal and said column selection circuit for the transfer of data and operatively connected to said clock input terminal for controlling the transferred timing;

a latch operatively connected between said data input terminal and said column selection circuit for the transfer of data and operatively connected to said clock input terminal for controlling the transferred timing;

latch means operatively connected between said chip select input terminal and said means for receiving and outputting, and connected to receive the clock from said clock input terminal;

latch means operatively connected between said enable input terminal and said column selection circuit, and connected to receive the clock [form] *from* said clock input terminal;

said means for receiving and outputting including a control circuit connected to said clock input terminal for receiving the clock, connected to said chip select input terminal for receiving the chip select signal through the corresponding latch means, outputting a row address set signal, and outputting a column address set signal;

said means for receiving and outputting further including row latch means operatively connected to said address input terminal for receiving the multiplexed address signal and outputting only the row address signal in response to the row address set signal [form] *from* the control circuit to said row address decoder, and

said means for receiving and outputting further including column latch means operatively connected to said address input terminal for receiving the multiplexed address signal and outputting only the column address signal in response to the column address set signal from the control circuit to said column address decoder.

6. The semiconductor RAM of claim **5**, wherein said [control circuit] *means for receiving and outputting* consists of latch and logic elements.

7. The semiconductor RAM of claim **6**, wherein said [control circuit] *means for receiving and outputting* includes delay means for producing a delayed clock from the clock, first AND-gate means inputting the clock and a chip select signal and outputting the row address [et] *set* signal, second AND-gate means inputting the chip select signal and the clock for outputting the column address set signal.

8. The semiconductor RAM of claim **7**, wherein said first and second AND-gate means are operative on the opposite sign logic of the clock with respect to each other.

9. The semiconductor RAM of claim **7**, wherein said [control circuit] *means for receiving and outputting* further includes a latch operative to feed the chip select signal to only one of said first and second AND-gate means synchronized with the clock, and the other of said first and second AND-gate means receiving the chip select signal bypassing the latch.

10. The semiconductor RAM of claim **4**, wherein said means for receiving and [operating] *outputting* produces a row address set signal from only the clock and the chip select signal and further produces a column address set signal from only the clock and the chip select signal; and

first means for separating the row address from the multiplexed address signal and feeding the separated row address to said row address decoder in response to only the row address set signal, and second means for separating the column address from the multiplexed address signal and feeding the separated column address to said column address decoder in response to only the column address set signal.

11. The semiconductor RAM of claim **10** , wherein said [control circuit] *means for receiving and outputting* is responsive to the first operative [pule] *pulse* of the clock when the chip select signal indicates selection of the semiconductor RAM for outputting the row address set signal.

12. The semiconductor RAM of claim **11**, wherein said [control circuit] *means for receiving and outputting* is responsive to the second operative pulse of the clock when the chip select signal indicates selection of the semiconductor RAM for outputting the column address set signal.

13. The semiconductor RAM of claim **12**, wherein said [control circuit] *means for receiving and outputting* is responsive to the third operative pulse of the clock when the chip select signal indicates selection of the semiconductor RAM for again outputting the column address set signal to provide a page mode by merely extending the duration of the chip select signal.

14. The semiconductor RAM of claim **13**, wherein said [control circuit] *means for receiving and outputting* determines the operative pulse of the clock as an edge of each successive pulse of the clock.

15. A semiconductor memory chip, comprising:

an address input terminal for receiving an address signal having row and column addresses time multiplexed;

an input terminal for receiving a control signal that is selectively active;

a clock input terminal for receiving a clock having a single periodic succession of clock pulses;

a memory cell array;

a data output terminal connected to said memory cell array to output data from said memory cell *array*;

a row address decoder having a row address input and an output connected to said memory cell array;

a column address decoder having a column address input and an output connected to said memory cell array; and

demultiplexing means for receiving the multiplexed address signal from said address input terminal and the clock from said clock input terminal, and for outputting the row address to the input of the row address decoder separate from the column address and outputting the column address to the input of the column address decoder separate from the row address in response to only the timing of the clock when the control signal at said input terminal is active.

16. The semiconductor memory of claim **15**, further comprising:

a data input terminal connected to said memory cell array for receiving data for said memory cell;

a column selection circuit operatively connected between said memory cell array and each of said data output terminal, data input terminal and *demultiplexing* means for receiving and outputting;

an enable input terminal for receiving an enable signal to indicate a selection of one of a write operation and a read operation;

said column selection circuit including means responsive to said enable signal for controlling the data connection between said memory cell array and each of said data input terminal and data output terminal;

a latch operatively connected between said data output terminal and said column selection circuit for the transfer of data and operatively connected to said clock input terminal for controlling the transferred timing;

a latch operatively connected between said data input terminal and said column selection circuit for the transfer of data and operatively connected to said clock input terminal for controlling the transferred timing;

latch means operatively connected between said input terminal of the control signal and said *demultiplexing* means for receiving and outputting, and connected to receive the clock from said clock input terminal;

latch means operatively connected between said enable able input terminal and said column selection circuit, and connected to receive the clock from said clock input terminal;

said *demultiplexing* means for receiving and outputting including a control circuit connected to said clock input terminal for receiving the clock, connected to said input terminal for receiving the control signal through the

corresponding latch means, outputting a row address set signal, and outputting a column address set signal;

said *demultiplexing* means for receiving and outputting further including row latch means operatively connected to said address input terminal for receiving the multiplexed address signal and outputting only the row address signal in response to the row address set signal from the control circuit to said row address decoder, and

said *demultiplexing* means for receiving and outputting further including column latch means operatively connected to said address input terminal for receiving the multiplexed address signal and outputting only the column address signal in response to the column address set signal from the control circuit to said column address decoder.

17. The semiconductor memory of claim **16**, wherein said control circuit consists of latch and logic elements.

18. The semiconductor memory of claim **17**, wherein said control circuit includes delay means for producing a delayed clock from the clock, first AND-gate means inputting the clock and a chip select signal and outputting the row address set signal, second AND-gate means inputting the chip select signal and the clock for outputting the column address set signal.

19. The semiconductor memory of claim **18**, wherein said first and second AND-gate means are operative on the opposite sign logic of the clock with respect to each other.

20. The semiconductor memory of claim **17**, wherein said control circuit further includes a latch operative to feed the control signal to only one of said first and second AND-gate means synchronized with the clock, and the other of said first and second AND-gate means receiving the control signal bypassing the latch.

21. The semiconductor memory of claim **15**, wherein said *demultiplexing* means for receiving and [operating] *outputting* produces a row address set signal from only the clock and the control signal and further produces a column address set signal from only the clock and the control signal; and

first means for separating the row address from the multiplexed address signal and feeding the separated row address to said row address decoder in response to only the row address set signal, and second means for separating the column address from the multiplexed address signal and feeding the separated column address to said column address decoder in response to only the column address set signal.

22. The semiconductor memory of claim **21**, wherein said control circuit is responsive to the first operative [pule] *pulse* of the clock when the control signal is active for outputting the row address set signal.

23. The semiconductor memory of claim **22**, wherein said control circuit is responsive to the second operative pulse of the clock when the control signal is active for outputting the column address set signal.

24. The semiconductor memory of claim **23**, wherein said control circuit is responsive to the third operative pulse of the clock when the control signal is active for again outputting the column address set signal to provide a page mode by merely extending the duration of the chip select signal.

25. The semiconductor memory of claim **24**, wherein said control circuit determines the operative pulse of the clock as an edge of each successive pulse of the clock.

26. A semiconductor dynamic memory chip, comprising:

a dynamic type random access memory cell array:

an address input terminal to be supplied with address signals having time multiplexed row address signals and column address signals;

a row address latch having an input which is supplied with said row address signals from said address input terminal;

a column address latch having an input which is supplied with said column address signals from said address input terminal;

a first latch circuit having an input which is supplied with an external chip select signal and a latch timing control terminal which is supplied with an external clock signal having a continuous succession of clock pulses of constant period;

a second latch circuit having an input which is supplied with a write enable signal and a latch timing control terminal which is supplied with said external clock signal;

a data input latch circuit having a data input which is supplied with an external data, a latch timing control terminal which is supplied with said external clock signal and a data output terminal which is coupled with said dynamic type random access memory cell array;

a data output latch circuit having a data input which is coupled with said dynamic type random access memory cell array, an output timing control terminal which is supplied with said external clock signal and a data output terminal;

a row address decoder having an input which is coupled with an output of said row address latch and an output which is coupled with said dynamic type random access memory cell array; and

a column address decoder having an input which is coupled with an output of said column address latch and an output which is coupled with said dynamic type random access memory cell array,

wherein said row address latch latches said row address signals in response to said external chip select signal latched by said first latch circuit and to a first level change of said external clock signal, and

wherein said column address latch latches said column address signals in response to said external chip select signal latched by said first latch circuit and to a second level change which appears after said first level change of said external clock signal.

27. A semiconductor dynamic memory chip according to claim 26,

wherein said data input latch circuit latches an input data in synchronism with said second level change.

28. A semiconductor dynamic memory chip according to claim 26,

wherein said data output latch circuit outputs an output data in synchronism with a third level change which appears after said second level change of said external which appears after said second level change of said external clock signal.

29. A semiconductor dynamic memory chip according to claim 26,

wherein said data input latch circuit latches an input data in synchronism with said second level change, and

wherein said data output latch circuit outputs an output data in synchronism with a third level change which appears after said second level change of said external clock signal.

30. A semiconductor dynamic memory chip according to claim 29,

wherein said column address latch latches a column address in response to the third level change of said

external clock signal at which said data output latch circuit outputs the output data.

31. A semiconductor dynamic memory chip according to claim 29,

wherein said column address latch latches repeatedly column address signals in response to each of a plurality of level changes which appear after said first level change of said external clock signal under a state that said row address latch latches said row address signals in response to said first level change.

32. A semiconductor dynamic memory chip according to claim 31,

wherein said column address latch latches a column address in response to the third level change of said external clock signal at which said data output latch circuit outputs an output data.

33. A semiconductor dynamic memory chip according to claim 26,

wherein said external chip select signal has a predetermined low level, and

wherein said first level change and said second level change go from a low level to a high level.

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